NARROW BODY RAISED SOURCE/DRAIN METAL GATE MOSFET

TECHNICAL FIELD

[0001] The present invention relates to semiconductor devices and methods of manufacturing semiconductor devices. The present invention has particular applicability to double-gate devices.

BACKGROUND ART

[0002] The escalating demands for high density and performance associated with ultra large scale integration semiconductor devices require design features, such as gate lengths, below 100 nanometers (nm), high reliability and increased manufacturing throughput. The reduction of design features below 100 nm challenges the limitations of conventional methodology.

[0003] For example, when the gate length of conventional planar metal oxide semiconductor field effect transistors (MOSFETs) is scaled below 100 nm, problems associated with short channel effects, such as excessive leakage between the source and drain, become increasingly difficult to overcome. In addition, mobility degradation and a number of process issues also make it difficult to scale conventional MOSFETs to include increasingly smaller device features. New device structures are therefore being explored to improve FET performance and allow further device scaling.

[0004] Double-gate MOSFETs represent new structures that have been considered as candidates for succeeding existing planar MOSFETs. In several respects, the double-gate MOSFETs offer better characteristics than the conventional bulk silicon MOSFETs. These improvements arise in part because the double-gate MOSFET has

a gate electrode on both sides of the channel, rather than on only one side as in conventional MOSFETs. When there are two gates, the electric field generated by the drain is better screened from the source end of the channel. Also, two gates can control roughly twice as much current as a single gate, resulting in a stronger switching signal.

[0005] A FinFET is a recent double-gate structure that exhibits good short channel behavior. A FinFET includes a channel formed in a vertical fin. The FinFET structure may be fabricated using layout and process techniques similar to those used for conventional planar MOSFETs.

SUMMARY OF THE INVENTION

[0006] Implementations consistent with the present invention provide a double-gate MOSFET that includes a metal gate, a narrow body and raised source/drain area.

[0007] One aspect of the invention is directed to a semiconductor device comprising an insulator and a semiconductor layer formed on the insulator, the semiconductor layer including a fin portion corresponding to a channel of the semiconductor device. A source region is formed at a first end of the semiconductor layer. A height of the source region is higher than that of the fin. A drain region is formed at a second end of the semiconductor layer and has a higher than that of the fin. A metal gate region is formed to overlap at a top surface and at least one side surface of the fin.

[0008] Another aspect of the invention is directed to a method for forming a semiconductor device. The method includes forming a semiconductor layer on an insulator, forming a dummy gate structure over at least a portion of the semiconductor layer and a portion of the insulator; and etching the semiconductor device to remove

the dummy gate structure and to create an area previously occupied by the dummy gate structure. The method also includes etching the semiconductor device to decrease a width and height of the semiconductor layer in an area corresponding to a fin structure of the semiconductor device, and depositing a metal layer in the area previously occupied by the dummy gate structure, the metal layer forming a gate for the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Reference is made to the attached drawings, wherein elements having the same reference number designation may represent like elements throughout.

[0010] Fig. 1A is a cross-section of exemplary layers used to form a semiconductor device formed in accordance with an embodiment of the invention;

[0011] Fig. 2B is a perspective view of the semiconductor device shown in Fig. 1A;

[0012] Fig. 2A is a top-view illustrating an additional stage in the formation of the semiconductor device;

[0013] Fig. 2B is a cross-section taken along the line A-A' in Fig. 2A;

[0014] Fig. 3 is a cross-section illustrating a further stage in the formation of the semiconductor device shown in Fig. 2B;

[0015] Fig. 4 is a cross-section illustrating a silicide material formed in a further stage in the formation of the semiconductor device shown in Fig. 3;

[0016] Fig. 5 is a cross-section illustrating a further stage in the formation of the semiconductor device shown in Fig. 4;

[0017] Fig. 6 is a cross-section illustrating planarization of the semiconductor device shown in Fig. 5;

[0018] Fig. 7 is a cross-section illustrating the semiconductor device of Fig. 6 after removal of a dummy gate structure;

[0019] Fig. 8 is a cross-section taken along the line B-B' in Fig. 2A after removal of the dummy gate structure;

[0020] Fig. 9A schematically illustrates a top view of the semiconductor device after performing an additional etch;

[0021] Fig. 9B is a cross-section taken along the line C-C' in Fig. 9A after removal of the dummy gate structure;

[0022] Fig. 10A is a cross-section illustrating a further stage in the formation of the semiconductor device of Fig. 9B;

[0023] Fig. 10B schematically illustrates a top view of the semiconductor device shown in Fig. 10A; and

[0024] Figs. 11A-11C are perspective diagrams illustrating formation of a nanowire.

BEST MODE FOR CARRYING OUT THE INVENTION

[0025] The following detailed description of the invention refers to the accompanying drawings. The same reference numbers may be used in different drawings to identify the same or similar elements. Also, the following detailed description does not limit the invention. Instead, the scope of the invention is defined by the appended claims and equivalents.

[0026] A FinFET, as the term is used herein, refers to a type of MOSFET in which a conducting channel is formed in a vertical Si "fin."

[0027] Implementations consistent with the present invention provide FinFET devices and methods of manufacturing such devices. The gates in the FinFET devices

formed in accordance with the present invention may include a metal. The source/drain regions may be raised relative to the channel of the FinFET. This device structure exhibits reduced series resistance and thus improved transistor drive current.

[0028] Fig. 1A illustrates a cross-section of a semiconductor device 100 formed in accordance with an embodiment of the present invention. Referring to Fig. 1A, semiconductor device 100 may include a silicon on insulator (SOI) structure that includes a silicon substrate 110, a buried oxide layer 120 and a silicon layer 130 formed on the buried oxide layer 120. Buried oxide layer 120 and silicon layer 130 may be formed on substrate 110 in a conventional manner.

[0029] In an exemplary implementation, buried oxide layer 120 may include a silicon oxide and may have a thickness ranging from about 1000 Å to about 3000 Å. Silicon layer 130 may include monocrystalline or polycrystalline silicon having a thickness ranging from about 600 Å to about 1000 Å. Silicon layer 130 is used to form a fin, a source, and a drain structure for a double-gate transistor device, as described in more detail below.

[0030] In alternative implementations consistent with the present invention, substrate 110 and layer 130 may include other semiconducting materials, such as germanium, or combinations of semiconducting materials, such as silicon-germanium. Buried oxide layer 120 may also include other dielectric materials.

[0031] Silicon layer 130 may be etched to form a rectangular active area. Fig. 1B is a perspective view illustrating semiconductor device 100, including the etched silicon layer 130. In an exemplary implementation, silicon layer 130 may be etched in a conventional manner, with the etching terminating on buried oxide layer 120 to form the rectangular silicon layer 130. As will be described in more detail below,

area 121 of silicon layer 130 will eventually become the source region of the semiconductor device and area 125 will eventually become the drain region.

[0032] A dummy gate structure may next be deposited, patterned, and etched on semiconductor device 100. Fig. 2A is top view illustrating a dummy gate structure 220 that extends over a middle area of silicon layer 130. This middle area will eventually be the channel of the semiconductor device. Dummy gate structure 220 may be formed from a polysilicon layer that may be deposited using conventional chemical vapor deposition (CVD) or other well known techniques. The polysilicon layer may be etched in a conventional manner to form the resultant structure 220 shown in Fig. 2A. Fig. 2B is a cross-section taken along the line A-A' in Fig. 2A.

[0033] Fig. 3 is a cross-section taken along the line A-A' in Fig. 2A illustrating a further stage in the formation of semiconductor device 100. A spacer material may be deposited adjacent dummy gate structure 220 and etched to form sidewall spacers 301. Sidewall spacers 301 may include, for example, an oxide material, and may range from about 150 Å to about 1000 Å. A metal layer may next be deposited on semiconductor device 100. The metal layer may be, for example, tungsten, cobalt, titanium, tantalum, or molybdenum. The metal layer may then be thermally annealed to create a metal silicide compound in the exposed silicon areas of silicon layer 130. Fig. 4 illustrates the resultant silicide material 402 after silicidation. Silicide material 402 may extend over the source region 121 and the drain region 125.

[0034] Fig. 5 is a cross-section illustrating a further stage in the formation of semiconductor device 100. As illustrated, a surrounding protective layer 501 may be deposited over semiconductor device 100. In one implementation consistent with the principles of the invention, surrounding layer 501 may include a dielectric material such as tetraethyl orthosilicate (TEOS), although other dielectric materials may be

used. Surrounding layer 501 may be deposited to a thickness of about 1500 Å to about 3000 Å.

[0035] As shown in Fig. 6, surrounding layer 501 may be planarized through a process such as chemical mechanical polishing (CMP). CMP is a know planarization technique that may be used to planarize a semiconductor surface. In one implementation, the planarization is performed until the upper surface of dummy gate structure 220 is exposed.

[0036] Surrounding layer 501 may next be used as a protective layer for the removal of dummy gate structure 220. In particular, semiconductor device 100 may be etched via an isotropic wet etch using a material that does not remove surrounding layer 501 or sidewall spacers 301, but removes the polysilicon of dummy gate structure 220. Fig. 7 is a cross-section illustrating semiconductor device 100 after removal of dummy gate structure 220.

[0037] The isotropic wet etch described above, in addition to removing dummy gate structure 220, may also remove portions of silicon layer 130 that are below dummy gate structure 220. Fig. 8 is a cross-section taken along the line B-B' in Fig. 2A after removal of dummy gate structure 220. The presence of dummy gate structure 220 and silicon layer 130 prior to the isotropic wet etch are shown in Fig. 8 by dashed lines 220' and 130', respectively. Due to the wet etch, dummy gate structure 220 is removed and silicon layer 130 is reduced. In particular, as shown in Fig. 8, the width of silicon layer 130 in the channel region of semiconductor device is reduced. The portions of silicon layer 130 outside of the channel region are protected by spacers 301 or protective layer 501 and are thus not reduced. The reduced portion of silicon layer 130 forms the fin of semiconductor device 100.

[0038] Consistent with an aspect of the invention, an additional etch of silicon fin 130 may next be performed. In one implementation, the exposed portion of silicon fin 130 may be etched to remove about 100 Å to about 300 Å of silicon fin 130. Fig. 9A schematically illustrates a top view of semiconductor device 100 after the additional etch of silicon fin 130. Fig. 9B is a corresponding cross-sections of Fig. 9A taken along the line C-C' in Fig. 9A. As shown, the width of the active area (i.e., the channel portion) of semiconductor device 100 is decreased from the whole width of silicon layer 130 to T_{fin}. In an exemplary implementation, T_{fin} may range from about 50 Å to about 500 Å. Also, the height of the active area of semiconductor device 130 is reduced to height d_1 from the height d_2 of the source and drain regions of the semiconductor device. Height d_1 may be, for example, about 500 Å to about 700 Å and d_2 may be about 600 Å to about 1000 Å.

[0039] Fig. 10A is a cross-section taken along line C-C' illustrating a further stage in the formation of semiconductor device 100. A metal layer 1003, such as, for example, tungsten, titanium, nickel, TaSiN, or TaN may be deposited on semiconductor device 100. Metal layer 1003 fills the recessed area corresponding to the removed dummy gate structure 220. Metal layer 1003 may then be planarized using a CMP process to the level of surrounding layer 501. The TEOS layer 501 may then be removed. The resulting semiconductor device 100, including the planarized metal layer 1003, is shown in Fig. 10A. A top-view of semiconductor device 100 is shown in Fig. 10B. As shown, metal layer 1003 has replaced dummy gate structure 220 as the gate for the semiconductor device 100. The raised and wider source/drain areas 121 and 125 reduce series resistance of semiconductor device 100, thereby improving transistor drive current.

OTHER IMPLEMENTATIONS

[0040] Multiple ones of the semiconductor devices illustrated above, along with other semiconductor devices, may be connected on a single chip using conductive lines. In one implementation, nanowires may be formed to implement some or all of these lines.

[0041] Fig. 11A is a perspective diagram illustrating formation of a nanowire. As shown, a semiconductive layer, such as Si, Ge, or SiGe is deposited and patterned to form a column 1101. Column 1101 may be formed above a base layer 1105, such as a buried oxide layer, that is etched to remove most of base layer 1105 except for a portion of the base layer 1105 under column 1101. As shown in Fig. 11B, a thin sacrificial oxide layer 1102 may then be formed around column 1101. The device may then be etched, as shown in Fig. 11C, to remove the base layer 1105. Accordingly, column 1101 is thus suspended based on its end connections and can function as a nanowire. The nanowire may be, for example, 1-10 nanometers in width *(w)*.

CONCLUSION

[0042] The FinFET described above includes a metal gate and relatively wide source/drain regions that are raised above the channel area of the FinFET. The resultant FinFET has a reduced series resistance and thus has an improved transistor drive current.

[0043] In the previous descriptions, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., in order to provide a thorough understanding of the present invention. However, the present invention can be practiced without resorting to the specific details set forth herein. In other

instances, well known processing structures have not been described in detail, in order not to unnecessarily obscure the thrust of the present invention.

[0044] The dielectric and conductive layers used in manufacturing a semiconductor device in accordance with the present invention can be deposited by conventional deposition techniques. For example, metallization techniques, such as various types of chemical vapor deposition (CVD) processes, including low pressure chemical vapor deposition (LPCVD) and enhanced chemical vapor deposition (ECVD) can be employed.

[0045] The present invention is applicable in the manufacturing of semiconductor devices and particularly in semiconductor devices with design features of 100 nm and below, resulting in increased transistor and circuit speeds and improved reliability. The present invention is applicable to the formation of any of various types of semiconductor devices, and hence, details have not been set forth in order to avoid obscuring the thrust of the present invention. In practicing the present invention, conventional photolithographic and etching techniques are employed and, hence, the details of such techniques have not been set forth herein in detail.

[0046] Only the preferred embodiments of the invention and a few examples of its versatility are shown and described in the present disclosure. It is to be understood that the invention is capable of use in various other combinations and environments and is capable of modifications within the scope of the inventive concept as expressed herein.